Curvature Wavefront Sensor
Arbitrary Waveform Generator

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**Without AO**
- Earth’s atmosphere distorts light
- Telescope images blurred

**With AO**
- Removes effects of atmospheric distortion
- Image resolution improved
AO System Components

- Science Instrument
  - Infrared
  - Visible
- Visible + IR Light (from target)
- Beam Splitter
- Wavefront Sensor
- Electric Signals
- Deformable Mirror
- Incoming perturbed wavefronts
- Outgoing corrected wavefronts
- Deformable mirror
Visible light reflects off one side of membrane

APDs count photons in each lenslet

Measure light intensity

Calculate wavefront phase shift
What vibrates membrane?

Other side of membrane
Problem
Solution

• Design your own AWG!

• Use DAC40 board
  • Field Programmable Gate Array (FPGA)
  • Digital-to-Analog Converters (DACs)
AWG Specification

- Range of period – 100 Hz to 4 kHz
- Number of points – 1000
- Voltage resolution – 14 bits (DAC40 DACs)
- Update rate for new waveforms – 0.1 seconds (10 Hz)
Logic Block Diagram

AWG

Timing

Memory

A

B
Implement using Quartus II
Design Flow

Design Entry (VHDL) → Compilation → Simulation → Program Device

```vhdl
ARCHITECTURE behave OF memory IS
  SIGNAL wrir : STD_LOGIC;
  SIGNAL CT : STD_LOGIC;
  SIGNAL address : address_bus;
  SIGNAL data : data_bus;
  SIGNAL datall : data_bus;
  SIGNAL data : data_bus;
  SIGNAL reg_enable : STD_LOGIC;

--Timing signals
  SIGNAL count_ena : integer RANGE 0 TO 2047 := 1001; --3500 clock cycles
  SIGNAL count : integer RANGE 0 TO 127 := 102; --301 next_pws
  SIGNAL BOC_count : integer RANGE 0 TO 15 := 6; --5 BOCs
  SIGNAL name_pt : STD_LOGIC;
  SIGNAL BOC : STD_LOGIC;
  SIGNAL cnt0 : STD_LOGIC;
  SIGNAL waveform : STD_LOGIC;
BEGIN
  counter : lpm_counter
  GENERIC MAP (LPM_WIDTH => 10)
  PORT MAP (clock => clk, qr => q, en => en, q => address);
memory : std_logic_vector
  GENERIC MAP (WIDTH => 14, BITMAP => 10, ADDRESS_REG => "UNREGISTERED",
  LPM_FILE => "memSrly.nlf")
  PORT MAP (data => dataln, rdaddress => address, waddress => waddress,
  rdata => rdata, q => rdata, inclock => clk);
memory2 : std_logic_vector
  GENERIC MAP (WIDTH => 14, BITMAP => 10, ADDRESS_REG => "UNREGISTERED",
  LPM_FILE => "memSrly.nlf")
  PORT MAP (data => dataln, rdaddress => address, waddress => waddress,
  rdata => rdata, q => rdata, inclock => clk);
reg : lpm_reg
  GENERIC MAP (LPM_WIDTH => 14)
  PORT MAP (data => data, clock => clk, enable => reg_enable, q => dac_data);
--GENERATE TIMING
  next_pt_count : count 1600 clocks
  PROCESS (clk, count_out)
  BEGIN
    IF (clk = '1') AND (clk'EVENT) THEN
      IF (count_out = 16) THEN
        next_pt <= '1';
        count_out <= count_out + 1;
        ELSIF (count_out = 1) THEN
          count_out <= 16;
          next_pt <= '1';
        ELSE
          count_out <= count_out + 3;
          next_pt <= '0';
        END IF;
      END IF;
    END PROCESS;
    --EOC counter - counts 101 next_pts
    PROCESS (next_pt, count)
    BEGIN
      IF (next_pt = '1') AND (next_pt'EVENT) THEN
        IF (count = 101) THEN
          --...
        END IF;
      END IF;
    END PROCESS;
END-behave;
```
Simulate Design

Design Entry (VHDL) → Compilation → Simulation → Program Device
Conclusion

Dual-stroke waveform concept

- Efficient – Only 1 wavefront sensor
- Astronomical objects appear 2.5X brighter

In the Future

- Interface DAC40 to oscilloscope
- Test AWG
- Implement in next generation AO system
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